



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:

A. MORGENSHTEIN et al

Serial No.: 10/648,474

Filed: August 27, 2003

For: Logic Circuit and Method of
Logic Circuit Design

Examiner:

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Group Art Unit: 2819

Attorney
Docket: 26327

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

LETTER TO CHIEF DRAFTSMAN

Sir:

Pursuant to the Examiner's approval, please correct Figs. 19 and 20 as shown in red ink on the attached sheet.

Respectfully submitted,

Sol Sheinbein
Registration No. 25,457

Date: February 15, 2004



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FORMAL DRAWINGS

Sir:

We enclose herewith a new set of formal drawings (56 sheets) for the
above-identified patent application.

Respectfully submitted,

Sol Sheinbein
Registration No. 25,457

Date: February 15, 2004